D4C

DATA I/O

Service Phone (516) 499-0335 Dan Callahan

PROM PROGRAMMER
PROGRAM CARD SET

909-1063-4

025-1063-4 DATA I/O REV S AUG 78

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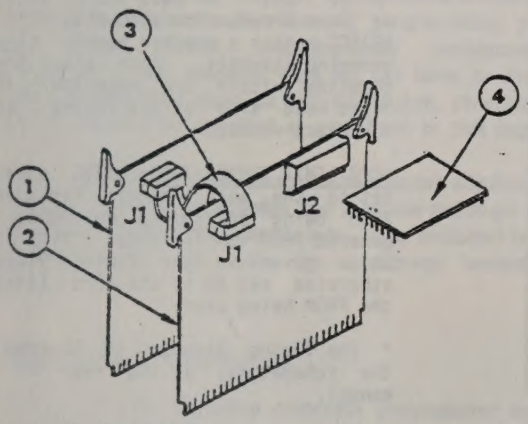
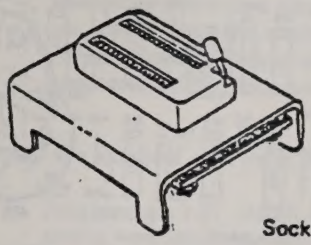
SPECIFICATION



1.	Digital Card	701-1225
2.	Analog Card	701-1063-4
3.	Interconnect Cable	709-1608
4.	Calib. Program Adapter	910-1063-4

Fig 1-1. Program Card Set 909-1063-4



Socket Adapter

Table 1-1. PROM types to Data I/O Socket Adapters

Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
HARRIS SEMICONDUCTOR				
32x8 FL	7602	VOL OC	16 PIN	1037
32x8 FL	7603	VOL TS	16 PIN	1037
256x4 FL	7610	VOL OC	16 PIN	1035-1
256x4 FL	7611	VOL TS	16 PIN	1035-1
512x4 FL	7620	VOL OC	16 PIN	1035-2
512x4 FL	7621	VOL TS	16 PIN	1035-2
512x8 FL	7640	VOL OC	24 PIN	1033-2
512x8 FL	7641	VOL TS	24 PIN	1033-2
512x8 FL	7647R	VOL TS	24 PIN	1411-2
1024x4 FL	7642	VOL OC	18 PIN	1039-3
1024x4 FL	7643	VOL TS	18 PIN	1039-3
1024x4 FL	7644	VOL OC	16 PIN	1042
1024x8 FL	7608	VOL TS	24 PIN	1033-3

DESCRIPTION

Program (Personality) Card Set 909-1063-4, with the appropriate Socket Adapter, provides Data I/O PROM programmers with the capability of programming and reading the PROMs listed in Table 1-1. Socket Adapters are available for each PROM listed. Table 1-1 references the Socket Adapters required to program (or read) the various PROMs.

INSTALLATION

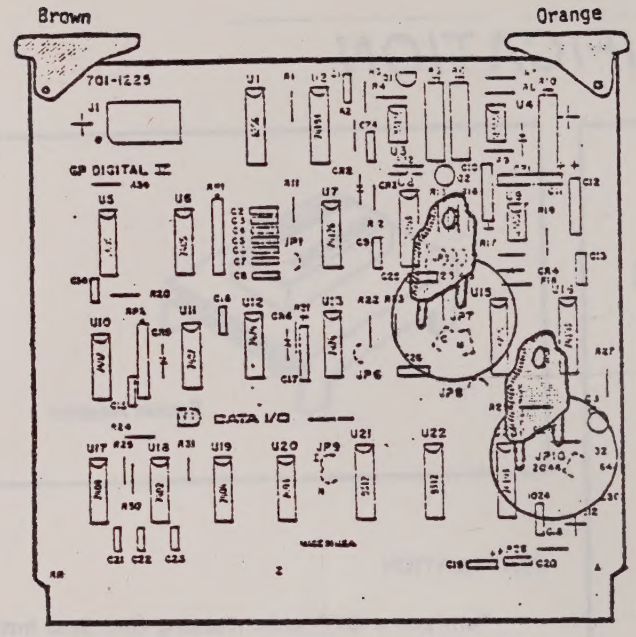
Turn power OFF while changing Card Sets. Install the Digital Card in programmer Brown-Orange card slot; install the interconnected Analog Card in White-White card slot. Component sides of cards should face forward in programmer Models 1-5, to the right in programmer satellites, and down in programmer Models 7 and 9. Connect J2 on Analog Card to front panel Socket Receptacle. Refer to the programmer manual for more detailed installation instructions.

CALIBRATOR PROGRAM ADAPTER

Program Card Set 909-1063-4 includes Calibrator Program Adapter 910-1063-4, which mates with the Data I/O Universal Calibrator. As shipped, this Program Card Set is precalibrated according to Data I/O Calibration Procedure 017-1063-4, which is included in the Performance Check Section of this manual.

CALIBRATION AND PERFORMANCE CHECK

Card Set calibration and performance verification procedures are given in the following pages. Calibration should be performed every 90 days, or if PROM programming yields fall below PROM manufacturers' recommendations. Performance Check should be performed after each calibration.

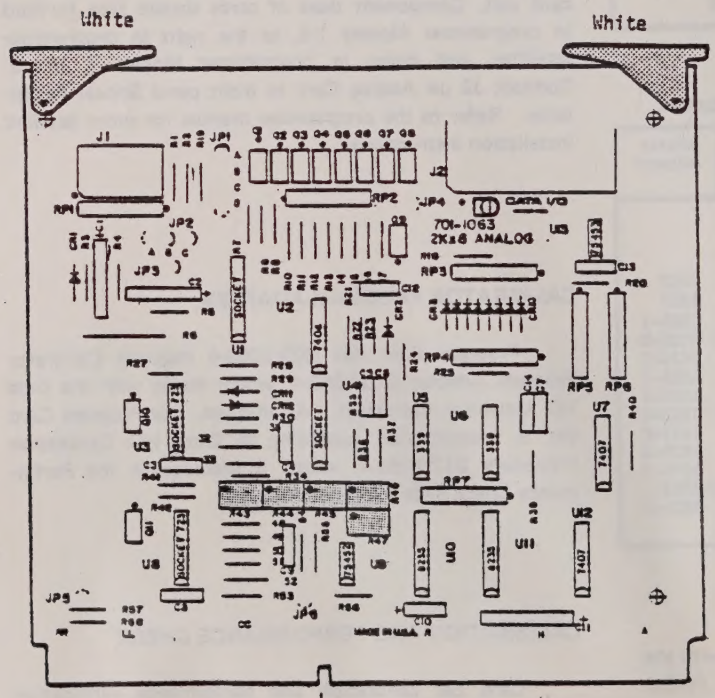


JUMPER POSITIONS, DIGITAL CARD

REJECT JUMPER JP7: JP7 sets the number of programming attempts before a REJECT is signaled to the programmer; select "M" or "C". "M" sets REJECT after one or more programming attempts; "C" sets REJECT after a greater number of programming attempts. Both values are determined within the Mode ROM. See the right hand side of the Timing Diagram* for exact values.

WORD LIMIT JUMPER JP10: JP10 should be set to the word (address) limit of the PROM being programmed or read. For generic PROM families, set JP10 at the value given in the Timing Diagram*, otherwise set it at the word limit of the PROM being used.

* The Timing Diagram is located with the schematics, at the rear of this manual.



Slot Registration for
Programmer 9

ADJUSTMENT LOCATIONS, ANALOG CARD

Adjustment locations are shown shaded. These adjustments are made during Calibration, as explained in the following section.

CALIBRATION/PERFORMANCE CHECK

INTRODUCTION

Since PROM manufacturers' shipments can vary from lot to lot, slight variations in PROM programming yields are to be expected. However, each manufacturer usually specifies certain minimum PROM programming yields—provided that specific approved programming techniques are employed. Data I/O Programmers employ manufacturer-approved programming techniques: therefore, if programming yields diminish below PROM manufacturers' recommended minimums, or, if the program card set has been in use for more than ninety days since its last calibration, programmer performance should be checked as explained in this section.

The performance check includes calibration adjustments of program waveform amplitudes and includes go/no-go tests of all critical programming parameters. Also included in the performance check are tests on resistively loaded ac waveforms.

DATA I/O FIELD SERVICES

Data I/O, Inc. furnishes complete programmer repair and calibration services at regional Field Service Centers and at the Data I/O factory. Contact your local Data I/O representative for further information.

TEST EQUIPMENT REQUIRED

To perform a complete performance check, the following equipment is required:

1. Data I/O Universal Calibrator, P/N 910-1071.

2. A. Prog. 1, 2, 3, 5: Data I/O Extender Card, P/N 910-1136.
   B. Prog. 9: Data I/O Extender Fixture, P/N 910-1074.

3. Digital Voltmeter: Fluke Model 8000A, or equivalent

4. Adjustment Tool: A three-inch screwdriver

5. Dual Trace Oscilloscope: Tektronix 465, or equivalent

6. Programmers 1, 2, 3, 5 only: Data I/O 13 inch Interconnect Cable, P/N 709-1613.

7. Programmer 9 only: Data I/O Interconnect Cables, P/N 709-1613 and 709-2608.

8. Jumper wires approximately 12 inches in length.

INSTALLATION OF UNIVERSAL CALIBRATOR

The following installation procedure assumes that the Universal Calibrator is mated with the Extender Card and that programmer power is off. On Programmers 1, 2, 3, and 5, remove the top cover to expose the card cage. To expose the card cage on the Model 9, open the access opening on the front of the chassis.

1. Remove end of 26-conductor cable from analog card. Remove both cards (analog and digital) from Programmer (or Satellite) card cage.

2. Remove end of 16 conductor cable from digital card J1.

CAUTION

Connector pins are fragile; careless connector extraction may result in bent or broken pins. Use a suitable tool—like a small screwdriver—when removing connectors from their sockets.

3. Install the extender card (with the Universal Calibrator in place).
   A. Programmers 1-5: Install the extender card into the analog card slot (white-white).
   B. Programmer 9: Install extender fixture into digital card slot (brown- orange).

4. A. Programmers 1-5: Install the analog card of the program card set into the card slot on top of the extender board. Refer to Figure 1.
   B. Programmer Model 9: Install the analog card in front card slot. Refer to Figure 2. The components should face the Calibrator.

5. A. Programmers 1-5: Install the digital card in the digital slot in the programmer.
   B. Programmer 9: Install the digital card behind the analog card on top of the extender card.

6. Making sure that cable red stripes and connector pins 1 are properly oriented, connect the analog card to the Universal Calibrator as follows:
   A. Programmers 1-5: Connect J1 of the analog card to J1 of the Universal Calibrator using the strap between the analog and digital cards. Connect J2 of the analog card to J2 of the Universal Calibrator using the ribbon cable that connects the card set and the programmer.
   B. Programmer 9: Connect J1 of the analog card to J1 of the Universal Calibrator using the strap between the analog and digital cards. Using the 26-connector cable supplied with the Calibrator, connect J2 of the analog card to J2 of the Calibrator.

7. Plug Calibrator Program Adapter into PROGRAM ADAPTER SOCKET on Universal Calibrator.

CAUTION

Be sure that the four-digit portions of both part numbers are identical: i.e. Analog card 701-XXXX is part of program card set 909-XXXX, which is calibrated by calibrator program adapter 910-XXXX.

8. Connect DVM ground probe to GND test point at left side of Universal Calibrator.

This completes installation of the Universal Calibrator.

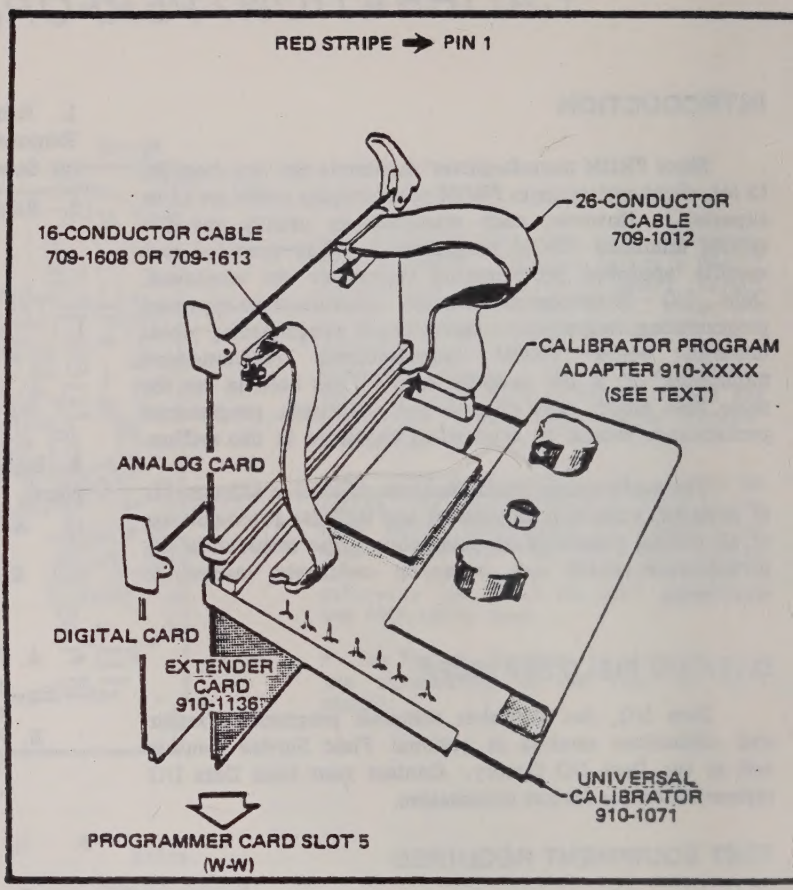


Figure 1. Installation of Universal Calibrator into Programmer Models 1, 2, 3, and 5 for Calibration/Performance Check.

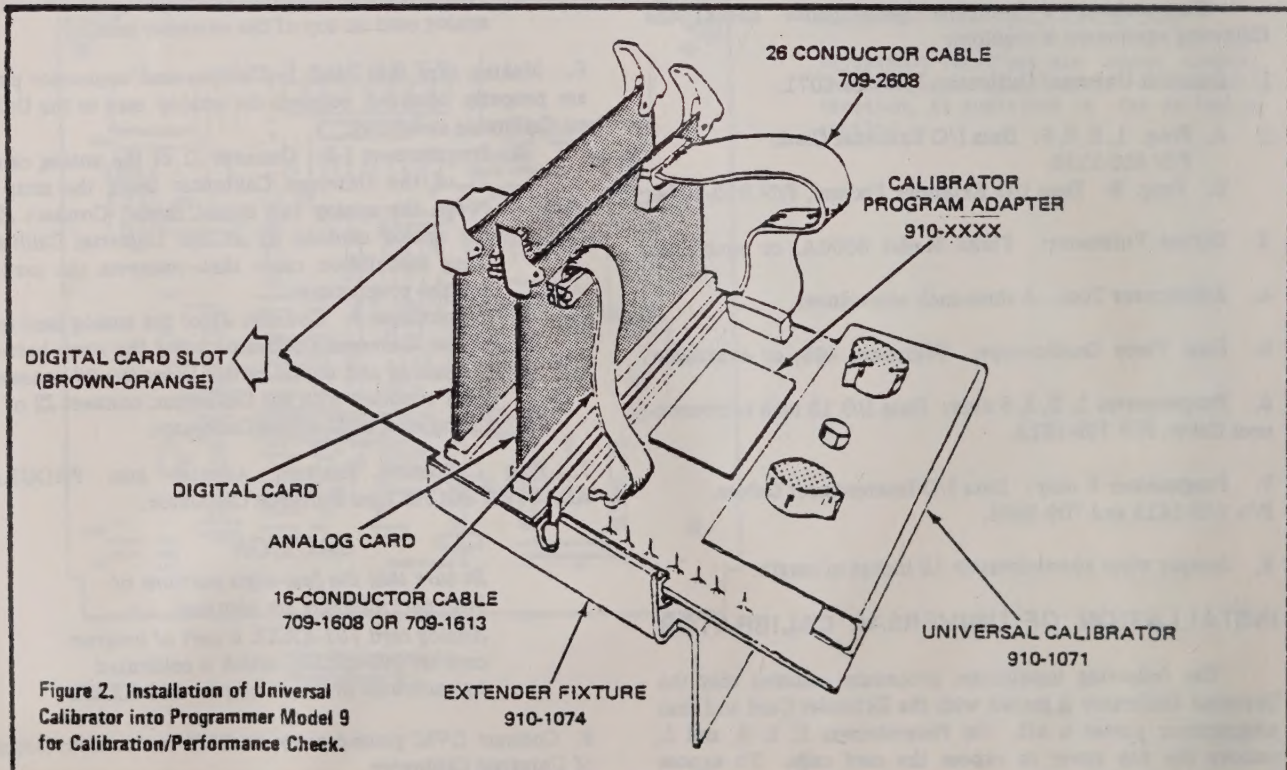


Figure 2. Installation of Universal Calibrator into Programmer Model 9 for Calibration/Performance Check.

CALIBRATION CHART

The calibration chart is to be used only with the (calibrator) program adapter specified in the title block of the chart.

The left-most portion of the chart contains truth tables for the calibrator program adapter. The truth tables are for documentation purposes only, and have no bearing on the actual performance check/calibration procedures.

PROGRAMMER WORD COUNT COLUMN is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When using the chart, refer to the address (word count) corresponding to the address readout configuration of the programmer in use. For instance, if your programmer has a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static (DC steady state) conditions created by the Universal Calibrator may cause thermal damage to compo-components if Programmer is left unattended with advanced word count.

TEST DESCRIPTION column contains three kinds of tests: (1) power supplies, (2) performance checks, and (3) calibration adjustments. The power supply tests are contained in the first five rows of the chart. (Note that power supply adjustments are located in the programmer, not in the program card set.) Performance checks fill the bulk of the Calibration Chart; these are characterized by min/max voltage limits only. No nominal (NOM) values are given, and no adjustments (ADJ) are prescribed.

Calibration steps are those with entries in the ADJ and NOM columns. These steps are evident by the note "CALIBRATION STEP" in the comments column.

SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load select switch; S3 is the line select switch. Generally, each step on the Calibration Chart requires changing of switch positions. S1 is push to test, and should be held depressed only long enough to obtain a DVM reading.

CAUTION

DO NOT hold S1 depressed for extended periods. Certain measurements induce high Programmer current levels. Extended high current operation (S1 depressed) may damage sensitive electronic components.

TEST POINT column gives test point location for DVM probe on Universal Calibrator. Some test points are located on the program card itself; for instance, if a test point is designated as U6 P8, it means that the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the comments column.

The ADJ column calls out potientiometer designations. The first four entries in the ADJ column refer to power supply potientiometers located on the power supply board of the Programmer. If adjustments are required, refer to Programmer manual. The remaining entries in the ADJ column refer to pots on the analog card. These are located as shown on page 1-2 in the Specifications section of this manual.

The LIMITS COLUMN is divided into three portions: MIN (minimum), NOM (Nominal), and MAX (Maximum). The values given are in volts, and indicate the range into which a given DVM reading should fall when S1 is pressed. If a reading is within the limits, no adjustment is required and the programmer (or program card set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (calibration steps), the card is non functional and should not be used for programming.

NOTES are written in a block at the bottom of the calibration chart. These apply to certain calibration steps and are referenced by numbers in the comments column. Notes called out by letter in the comments column apply only to Model IX calibration.

PERFORMANCE CHECK AND CALIBRATION PROCEDURE

DC CALIBRATION

The following paragraphs describe the method by which a program card set is checked/calibrated in conjunction with the applicable Calibration Chart. The procedure assumes that the Universal Calibrator is properly installed, as previously described. The following procedure should be performed with the programmer in an ambient temperature range between 15°C to 35°C.

Initialization

1. Switch Programmer power ON; allow Programmer to warm up for approximately five minutes.
2. Programmers 1, 2, 3, and 5:
   Press: RESET
   ROM2-ROM2
   MANUAL
   PROGRAM
   START

   Programmer 9:
   Press: EXECUTE
   Set NORMAL/INVERT switch to INVERT.

Power Supply

During the procedure the programmer card cage should contain all boards normally used.

Connect DVM between GND and the Universal Calibrator test points given in Steps 1-1 through 1-5 on the Calibration Chart. Measured voltages should fall within the given limits. (Calibrator Switch positions do not matter.)

If any power supply voltage measurement reading is outside of the given range, adjustment must be made. Power supply adjustments are located on the power supply board within the Programmer.

If a Programmer Satellite is being used, check/calibrate Satellite power supply as explained in Satellite Manual.

Performance Check/Calibration

1. Use FWD and REV keys on Programmer keyboard to index the "address display" (word count) to the decimal (DEC), hexadecimal (HEX), or octal (OCT) address given in the word count column of the calibration chart.

CAUTION

DO NOT leave Word Count advanced beyond 000 for extended periods. Static (DC steady state) conditions created by the Universal Calibrator may cause thermal damage to components if Programmer is left unattended with advanced word count. Press Reset to relieve possible thermal stresses.

2. With Word Count set, and DVM probes installed between GND and the indicated test point on the universal calibrator, set switches S2 and S3 to the positions indicated. Press S1 to test.

CAUTION

DO NOT hold S1 depressed for extended periods. Certain measurements induce high current levels within the Programmer. Extended high current operation (S1 depressed) puts unnecessary stress on sensitive electronic components.

3. While S1 is held, DVM readings should fall between the indicated limits for each measurement. If a DVM reading is outside of limits, or if the reading cannot be adjusted to fall within limits (ADJ column), DO NOT use the card set for programming.

Proceed through the Calibration Chart until all tests have been performed. At the conclusion of testing, turn Programmer power OFF, and proceed to AC Dynamic Tests.

AC CALIBRATION

AC Dynamic Tests

The following procedure is used to obtain the "Program Waveforms" shown on the Timing Diagram at the rear of this manual.

These waveforms, indicated by circled digits (①,②,③,..) on the timing diagram, are identically referenced on the Calibration Chart. The waveforms are obtained by selecting switch positions (S2 and S3) on the Universal Calibrator and feeding the selected signals to an appropriately triggered dual trace oscilloscope.

Test Set-Up

1. Make sure that programmer power is Off.

2. A. Programmers 1-5: Remove the digital card from the cage. Refer to Figure 3.
   B. Programmer 9: Remove the digital card from the extender. Refer to Figure 4.

3. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

4. A. Programmers 1-5: Disconnect the other end of the 16-conductor cable from J1 of the analog card. Substitute the 13 inch cable supplied with the Calibrator and connect J1 of the analog card to J1 of the digital card.
   B. Programmer 9: Connect the free end of the 16-conductor cable to digital card J1, assuring that cable red stripe and connector pin 1 are properly oriented.

5. Connect triggered input channel of dual trace oscilloscope to digital card test pulse. The location of the test pulse on the digital card is noted to the left of the Test waveform on the timing diagram. Connect the other channel to TP3 on the Calibrator. Re-install the digital card per step 2, above.

6. Using a suitable jumper cable, connect the Read Enable line emanating from analog card J1-16 to ground. (Use either the programmer chassis or the GND test point on the Universal Calibrator.)

7. Programmer 9: Set NORMAL/INVERT switch to INVERT.

CAUTION

Make sure that J1-16 is properly connected to ground. If it is inadvertently connected to any other potential, damage to Programmer components may result.

8. Turn Programmer power ON.

9. Programmers 1, 2, 3, 5:
   Press: RESET
   RAM-RAM
   PROGRAM
   MANUAL
   START
   Programmer 9:
   Press: KEYBOARD

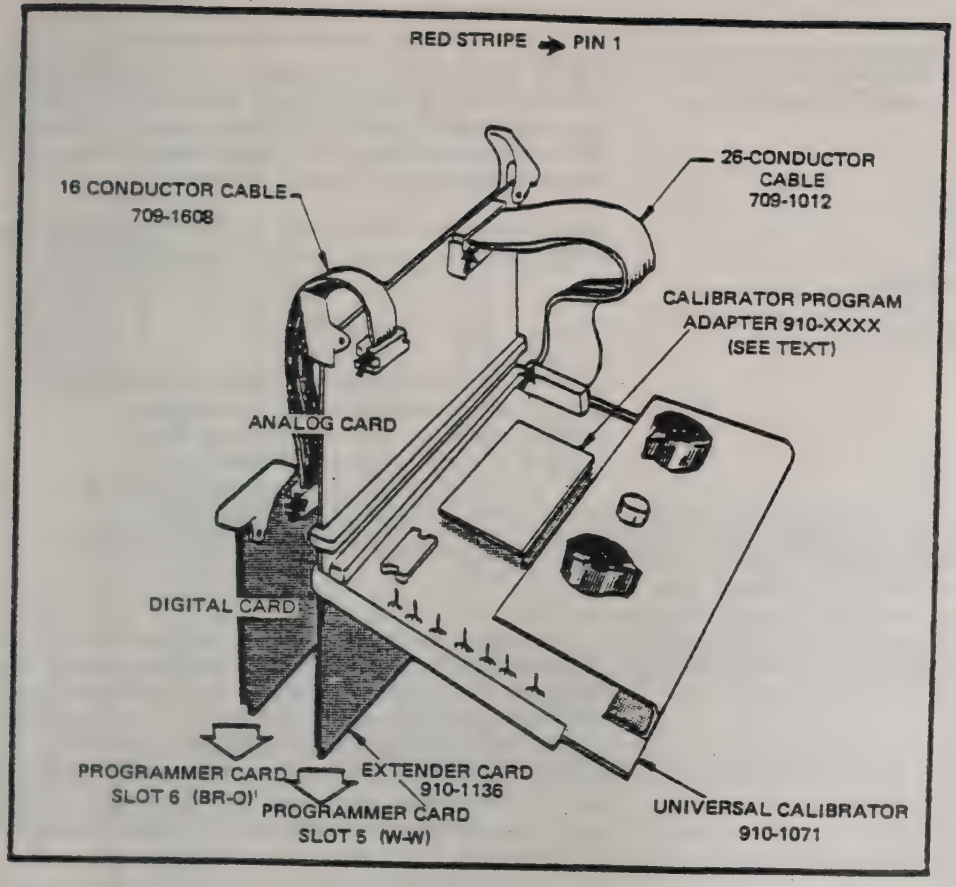


Figure 3. Installation of Universal Calibrator into Programmer Models 1, 2, 3, and 5 for AC Dynamic Tests.

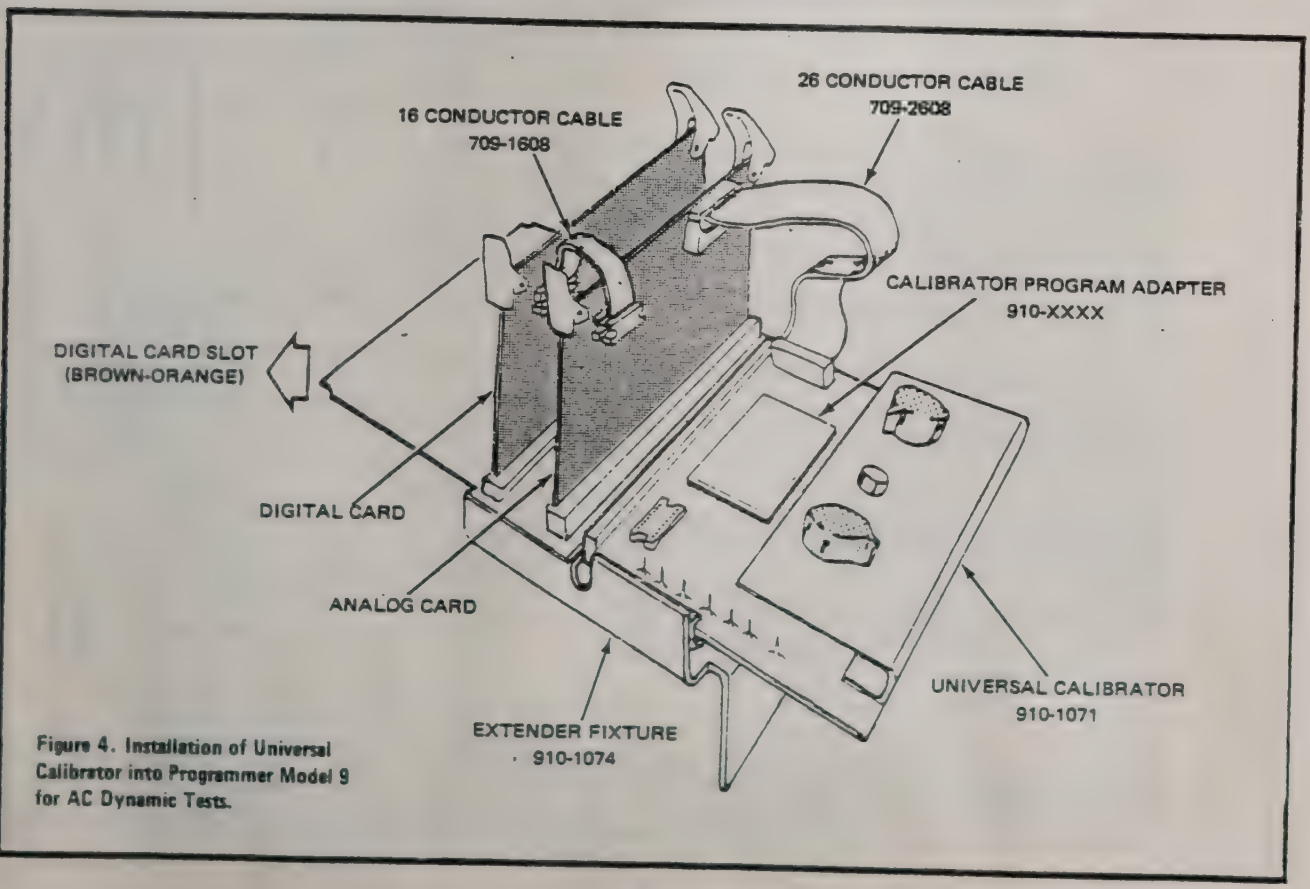


Figure 4. Installation of Universal Calibrator into Programmer Model 9 for AC Dynamic Tests.

10. Load approximately ten RAM addresses with bit 1 (only). This is accomplished by pressing 1 and FWD repetitively, or a tape may be used.

11. Programmers 1, 2, 3, 5:
Press: RESET
PROG
AUTO
RAM-ROM2

Programmer 9:
Press: PROGRAM

Waveform Observations

Initiate waveforms:
Programmers 1-5: press START.
Programmer 9: press EXECUTE.

The machine will stop on those addresses loaded in step 10 of the test set-up. If an abort condition is indicated, press WORD SKIP (SKIP on the Model 9) to advance the word count and repeat output of programming waveforms. An abort condition is indicated on Models 1, 2, 3, and 5 if the PROGRAMMING and INTERRUPT indicators come on. A Model 9 displays an abort condition by flashing the "P" indicator.

The "Program Waveforms" on the timing diagram at the rear of the manual are cross-referenced to the "Test Description" column on the Calibration Chart by circled digits (①, ②, ③ ...). To obtain the various waveforms use S2 and S3 on the Universal Calibrator to select the positions indicated in the "Switch Positions" column of the calibration chart and press S1 to test. S3 routes analog card output to TP3 (oscilloscope probe); S2 selects resistive loads, which are connected to ground when S1 is pressed.

NOTE: *All other information on the calibration charts is of no importance during waveform observations.*

CAUTION

When S1 is pressed high currents are induced within the Programmer; do not hold S1 depressed for extended periods. High currents are also present when the programmer is locked into program mode with advanced word count; RESET before leaving programmer unattended during these tests.

During these tests note that the Abort, Pause, and Reject functions of the program card set remain active; Press WORD SKIP to refresh the display. The abort timer signals a reject after a specific programming time. The pause timer controls the on/off time of the programming function. The position of the reject jumper (C or M) limits the number of applied programming pulses. Refer to the notes column of the timing diagram for definitions of the abort, pause, and reject functions.

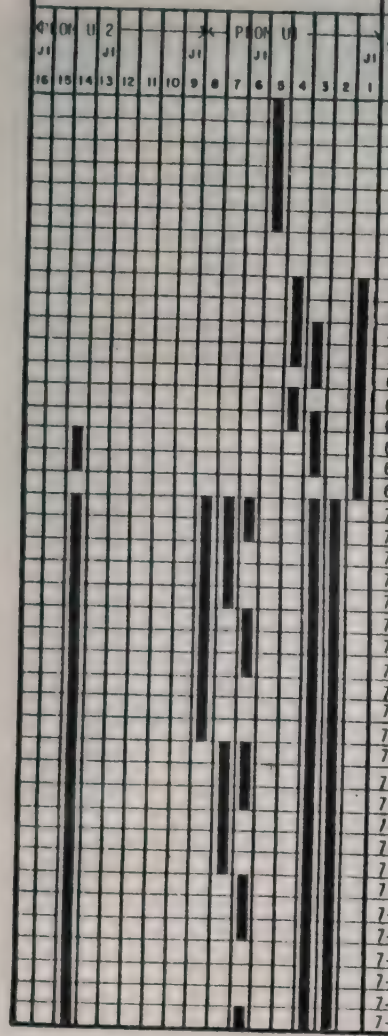
MANUAL
SEE SET UP ON PAGE 4.3 ON 909-919-1226-1
PAK PROGRAMMER
FOLLOW WRITTEN INSTRUCTION PAGE 4-4A

DATA I/O
REDMOND, WASH.

CALIBRATION CHART 017-1063-4
FIXTURE 702-1071
PROGRAM ADAPTER 910-1063-4
PROGRAM CARD 909-1063-4

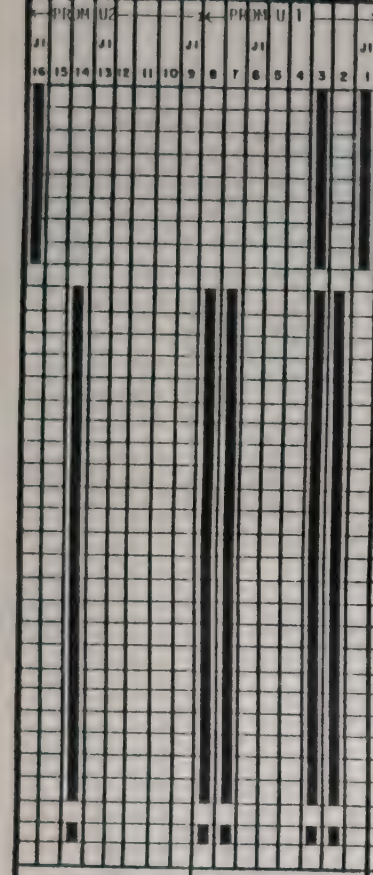
MANUFACTURE HARRIS
PROM HARRIS GENERIC FAMILY

DATE	SYM	REVISION RECORD	DR	CK
12-77	P	ECN #1977	DS	RT
3-78	-	ECN #2122	RT	RT
6-78	R	ECN #2313	KJ	RT
7-28-78	S	ECN #2369	DB	SC



STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	TEST DESCRIPTION	SWITCH POSITIONS S2	S3	MEASUREMENT PRESS S1 TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	COMMENTS
1-1	000	00	000				+24	R26	23.5	24.0	24.5	)
1-2	000	00	000	POWER			+48	R24	49.4	49.7	49.8	) ADJUSTMENTS LOCATED ON POWER SUPPLY BOARD.
1-3	000	00	000	SUPPLY			+ 5	R18	5.05	5.10	5.15	) SEE PROGRAMMER MANUAL.
1-4	000	00	000				- 9	R40	-9.2	-9.0	-8.8	)
1-5	000	00	000				PROG V		15.5		17.5	
2-1	000	00	000	$\overline{CP}$ VIH	3	6	TP3		2.4		2.7	
2-2	001	01	001	$\overline{CP}$ VIL	10	6	TP3		0.0		0.4	
3-1	001	01	001	$\overline{CE2}$ VIH (2)	2	5	TP3		2.4		2.7	
3-2	002	02	002	$\overline{CE2}$ VIL	10	5	TP3		0.0		0.4	
4-1	002	02	002	COMPARATOR REFERENCE (FWD)	-	-	U6-6		1.5		1.9	) TEST POINT LOCATED ON ANALOG CARD
4-2	003	03	003	COMPARATOR REFERENCE (REV)	-	-	U6-6		0.8		1.1	) TEST POINT LOCATED ON ANALOG CARD
5-1	003	03	003	$\overline{VOL}$/VOH	3	7	TP3		2.4		2.7	
6-1	004	04	004	VCC READ	5	1	TP3	R46	4.8	5.0	5.2	Calibration Step
6-2	005	05	005	VCC VERIFY FWD	5	1	TP3	R47	5.2	5.5	5.7	Calibration Step
6-3	006	06	006	VCC VERIFY REV	5	1	TP3	R45	4.3	4.5	4.7	Calibration Step
6-4	007	07	007	VCC PROGRAM (1)	5	1	TP3	R44	11.75	12.00	12.25	Calibration Step
6-5	007	07	007	ICC LIMIT	6	1	TP3		9.5		12.0	
6-6	008	08	010	VCC KILL	7	1	TP3		0.0		0.4	
7-1	009	09	011	BIT 8 VOP	7	8	TP3		11.75		12.25	
7-2	009	09	011	BIT 8 I LIMIT	5	8	TP3		2.0		2.8	
7-3	010	0A	012	BIT 8 DESELECT	8	8	TP3		0.0		0.4	
7-4	010	0A	012	BIT 7 VOP	7	9	TP3		11.75		12.25	
7-5	010	0A	012	BIT 7 I LIMIT	5	9	TP3		2.0		2.8	
7-6	011	0B	013	BIT 7 DESELECT	8	9	TP3		0.0		0.4	
7-7	011	0B	013	BIT 6 VOP	7	10	TP3		11.75		12.25	
7-8	011	0B	013	BIT 6 I LIMIT	5	10	TP3		2.0		2.8	
7-9	012	0C	014	BIT 6 DESELECT	8	10	TP3		0.0		0.4	
7-10	012	0C	014	BIT 5 VOP	7	11	TP3		11.75		12.25	
7-11	012	0C	014	BIT 5 I LIMIT	5	11	TP3		2.0		2.8	
7-12	013	0D	015	BIT 5 DESELECT	8	11	TP3		0.0		0.4	
7-13	013	0D	015	BIT 4 VOP	7	12	TP3		11.75		12.25	
7-14	013	0D	015	BIT 4 I LIMIT	5	12	TP3		2.0		2.8	
7-15	014	0E	016	BIT 4 DESELECT	8	12	TP3		0.0		0.4	
7-16	014	0E	016	BIT 3 VOP	7	23	TP3		11.75		12.25	
7-17	014	0E	016	BIT 3 I LIMIT	5	23	TP3		2.0		2.8	
7-18	015	0F	017	BIT 3 DESELECT	8	23	TP3		0.0		0.4	
7-19	015	0F	017	BIT 2 VOP (4)	7	22	TP3		11.75		12.25	
7-20	015	0F	017	BIT 2 I LIMIT	5	22	TP3		2.0		2.8	
7-21	016	10	020	BIT 2 DESELECT	8	22	TP3		0.0		0.4	
7-22	016	10	020	BIT 1 VOP (3)	7	21	TP3		11.75		12.25	
7-23	016	10	020	BIT 1 I LIMIT	5	21	TP3		2.0		2.8	
7-24	017	11	021	BIT 1 DESELECT	8	21	TP3		0.0		0.4	

FROM THIS POINT
<— PRESS S1 ON
UNIV CAL TO OBTAIN LIMITS



STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	TEST DESCRIPTION	SWITCH POSITIONS S2	S3	MEASUREMENT PRESS S1 TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
8-1	018	012	022	BIT 8 COMPARATOR	6	8					
8-2	018	012	022	BIT 7 COMPARATOR	6	9					
8-3	018	012	022	BIT 6 COMPARATOR	6	10					
8-4	018	012	022	BIT 5 COMPARATOR	6	11					
8-5	018	012	022	BIT 4 COMPARATOR	6	12					
8-6	018	012	022	BIT 3 COMPARATOR	6	23					
8-7	018	012	022	BIT 2 COMPARATOR	6	22					
8-8	018	012	022	BIT 1 COMPARATOR	6	21					
9-1	682	2AA	1252	A0 VIL (5)	3	20	TP3		0.0		0.4
9-2	682	2AA	1252	A1 VIH	3	19	TP3		2.4		2.7
9-3	682	2AA	1252	A2 VIL	3	18	TP3		0.0		0.4
9-4	682	2AA	1252	A3 VIH	3	17	TP3		2.4		2.7
9-5	682	2AA	1252	A4 VIL	3	16	TP3		0.0		0.4
9-6	682	2AA	1252	A5 VIH	3	15	TP3		2.4		2.7
9-7	682	2AA	1252	A6 VIL	3	14	TP3		0.0		0.4
9-8	682	2AA	1252	A7 VIH	3	13	TP3		2.4		2.7
9-9	682	2AA	1252	A8 VIL	3	2	TP3		0.0		0.4
9-10	682	2AA	1252	A9 VIH	3	3	TP3		2.4		2.7
9-11	682	2AA	1252	A10 VIL	3	4	TP3		0.0		0.4
9-12	1365	555	2525	A0 VIH	3	20	TP3		2.4		2.7
9-13	1365	555	2525	A1 VIL	3	19	TP3		0.0		0.4
9-14	1365	555	2525	A2 VIH	3	18	TP3		2.4		2.7
9-15	1365	555	2525	A3 VIL	3	17	TP3		0.0		0.4
9-16	1365	555	2525	A4 VIH	3	16	TP3		2.4		2.7
9-17	1365	555	2525	A5 VIL	3	15	TP3		0.0		0.4
9-18	1365	555	2525	A6 VIH	3	14	TP3		2.4		2.7
9-19	1365	555	2525	A7 VIL	3	13	TP3		0.0		0.4
9-20	1365	555	2525	A8 VIH	3	2	TP3		2.4		2.7
9-21	1365	555	2525	A9 VIL	3	3	TP3		0.0		0.4
9-22	1365	555	2525	A10 VIH	3	4	TP3		2.4		2.7
10-1	1365	555	2525	GROUND TEST	8	24	TP3		0.00		0.08
)	ALL WORDS NOT SHOWN										

CALIBRATION CHART 017-1063-4 **(CONTINUED)**
PAGE 2 OF 2

COMMENTS

7F
BF
DF
EF
F7
FB
FD
FE

P5: OBSERVE DO LIGHTS FOR SELECTED BIT ON, ALL OTHERS OFF.

P9: PRESS PROM KEY TO OBSERVE DATA AT LEFT

PROM U2 TRUTH TABLE	PROM U1 TRUTH TABLE
LINE = HI (1)	NO LINE=LOW(0)

CIRCUIT DESCRIPTION

CIRCUIT DESCRIPTION, PROGRAM CARD SET

INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 4-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses from the analog card until either ABORT or REJECT is signaled, or until the bit is programmed.

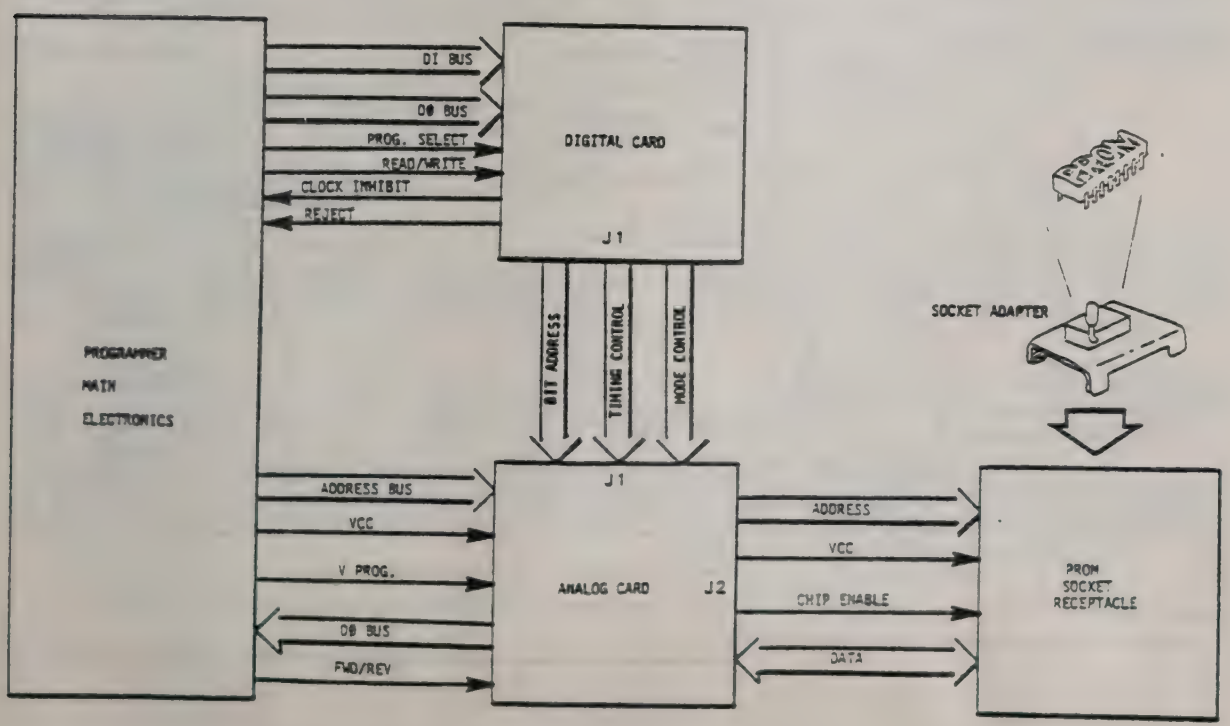
ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturer's specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow and timing. ROM truth tables, timing diagrams, jumper positions, and reject conditions are discussed. Detailed circuit schematics with timing diagrams and truth tables are found at the rear of this manual--refer to these for pin-out and interconnect information.

Fig. 4-1. Simplified Block Diagram of Program Card Set



CIRCUIT DESCRIPTION GP DIGITAL

BLOCK DIAGRAM

Figure 4-2 gives a generalized block diagram for the GP Digital Card. This diagram shows signal flow, and functional relationships between the blocks but does not include detailed interconnect information. Refer to the schematics and timing diagram (with truth tables) at the rear of this manual for details of circuit connection and operation. The following paragraphs discuss the functions contained on the digital card.

PROGRAM MEMORY

When the digital card is selected for operation, Program Memory will set upon receiving a Write command on AA. This causes the Clock Generator on the digital card to begin operation and halts the Programmer clock. Prior to setting of Program Memory, Program Pulse Counter, Bit Counter, and Sequence Counter are initialized, and Overprogram Counter is cleared.

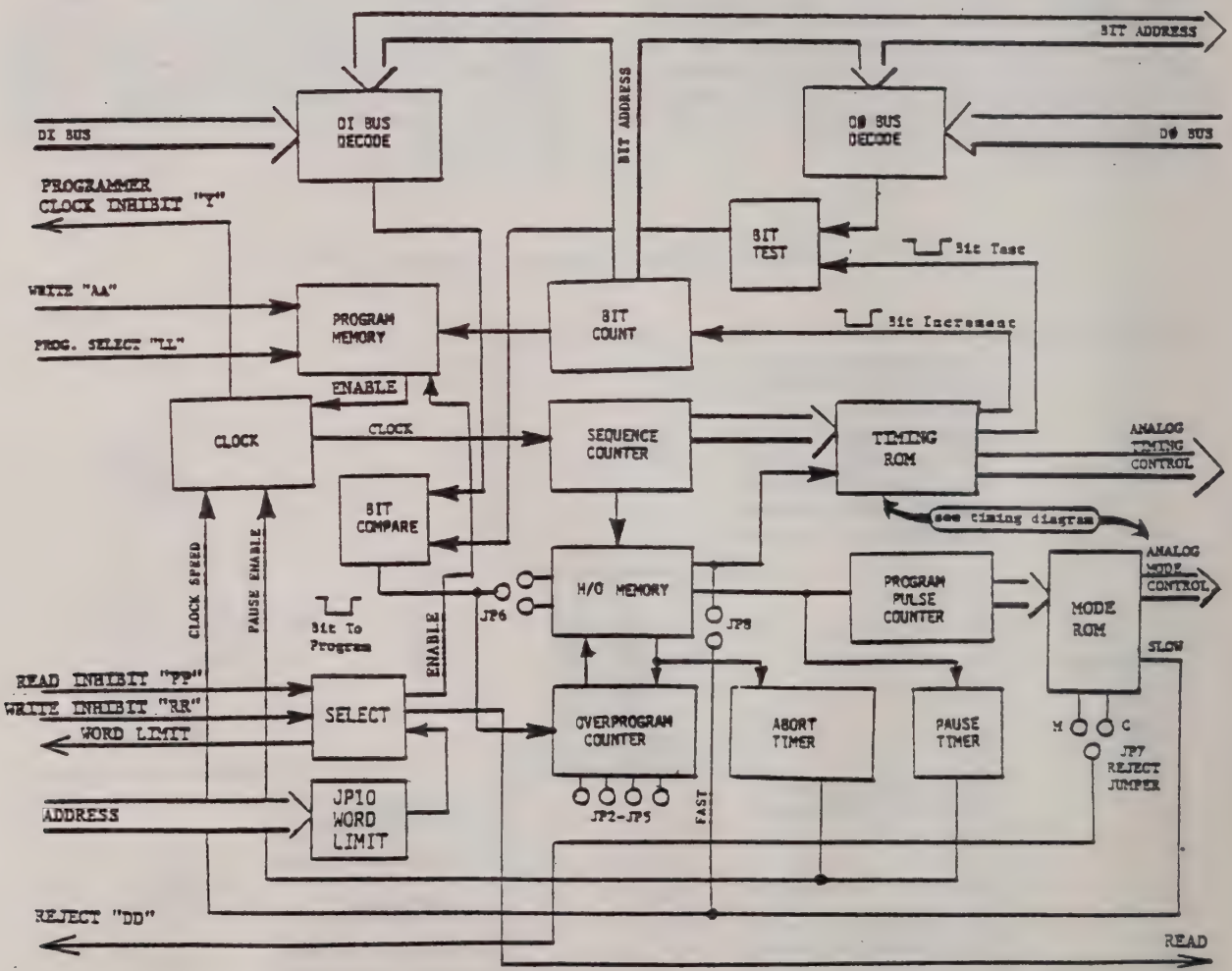
CLOCK GENERATOR

When Program Memory toggles in response to Write and Program Select commands, Clock Generator begins operation and the Programmer clock is inhibited. Clock pulses increment the Sequence Generator. Clock rate is determined by Mode and Timing ROM or by High Order Memory (with JP8 connected). The Clock may be halted by the Abort Timer, or by the Pause Timer (with CR2 connected).

SEQUENCE COUNTER AND TIMING PROM

The Sequence Generator consists of a 4-bit counter which drivers the 32x8 Timing ROM. The combination generates timing signals for analog control, along with Bit Test and Bit Increment pulses, which are used on the digital card (See Timing Diagram). A clock pulse is also output for PROMs with registers.

Fig. 4-2. Generalized Block Diagram for GP Digital Card



BIT COUNTER

The Bit Counter counts Bit Increment pulses arriving from the Timing ROM. Bit Increment pulses are counted, however, only when H/O Memory is enabled via a Bit to Program pulse from the Bit Compare gate. The Bit Counter counts down from either 4 or 8, as determined by input from the Analog Card or from the Mode ROM. Output from the Bit Counter controls the DO Bus Decoder and DI Bus Decoder. When the Bit Counter reaches zero, its borrow output is used to reset Program Memory.

PROGRAM PULSE COUNT AND MODE CONTROL

As program pulses are delivered to the PROM being programmed, the Program Pulse Counter counts up; outputs from the Program Pulse Counter are used as address line inputs to the Mode Control ROM. The Timing Diagram includes the truth table for the Mode Control ROM. Outputs of Mode ROM control the magnitude of program pulses (bits 1 and 2), along with clock speed (bit 3). Bits 4 and 5 control the number of programming attempts allowed before a reject is returned to the Programmer ; reject jumper JP7 selects either the M line or the C line (see Timing Diagram). M jumper sets the reject after one or more program attempts; C jumper rejects after multiple attempts, as determined in the Mode Control ROM.

TIMING PROM

Output words from the Timing ROM are used in the serial Verify and Program operations, as shown in the timing diagram. Verify operations utilize Low Order words 0 through 15; Program operations utilize High Order words 16 through 31. Words 8 through 11 are used to output control for Vcc voltages during Read and Verify operations. These operations occur under machine control when the digital card is not selected. At the beginning of a programming sequence (word 2), the Timing ROM outputs a Bit Test pulse to the Bit Test gate. If the DO Bus Decoder determines that there is no bit already programmed in the PROM, and if the DI Bus Decoder determines that there is a bit to program, then the Compare Gate outputs a Bit to Program pulse.

OVERPROGRAM COUNTER

The Bit to Program pulse arrives at the preset input of the H/O Memory, and at the load port of the Overprogram Counter. As H/O Memory is preset, the Bit Count Gate is disabled and remains so until the Overprogram Counter clocks H/O Memory after the bit has been programmed.

H/O MEMORY Word 15, the carry pulse from the Sequence Counter is allowed to toggle U13B (See Schematic). As U13B is toggled the fifth address line to the Timing ROM is enable, and it advances into High Order (Program) Count, words 16 through 31.

At word count 31, the Sequence Counter outputs another carry pulse to H/O Memory. The carry pulse toggles U13B, which sets the Timing ROM back to Low Order Count (Verify). At word 2, again, a Bit Test pulse is output from the Timing ROM; if the buses compare at Bit Test (bit is programmed), the output of Bit Compare gate remains unchanged (no Bit to Program), the H/O Memory remains enabled, and the Bit Count gate remains disabled.

At word 15 the Sequence Counter outputs another carry pulse which again causes High Order (Program) count, causing the Overprogram Counter to decrement. The above cycle repeats until the Overprogram Counter outputs a borrow pulse after counting down from the level preset by JP2-JP5. The borrow pulse clocks H/O Memory which enables the Bit Count gate, allowing it to decrement the Bit Count to the next bit.

Some digital cards are wired with JP6 shorted. If JP6 is shorted, Program Memory holds H/O Memory reset so that the Timing ROM jumps to High Order (Program Cycle) after Bit Test. When a Bit to Program pulse is received at (shorted) JP6, the fifth address input line to the Timing ROM goes high and H/O Memory is enabled. At Word 31, the carry pulse from the Sequence Counter shifts the count sequence back to Low Order. With JP6 shorted, the total sequence is 16 clock pulses long.

ABORT TIMER

The Abort Timer measures the time required to program a bit. If programming time is excessive, and JP1 is shorted, a REJECT is signaled and the clock is halted. The Abort Timer is connected to the Overprogram Counter such that an abort is possible only during Low Order count (Verify cycle).

PAUSE TIMER

The Pause Timer measures the time to program the PROM. A transistor is used in conjunction with the timing components to integrate out the time that the Program Memory is set. If programming time exceeds the value set by circuit components, the Clock is stopped in order to allow the PROM to cool; after a pause in the order of seconds the Clock is allowed to start again, and programming continues. Pause Timer output is gated with the Timing ROM so that a pause cannot occur during program pulses.

SELECT GATES

U17 and U18 (on schematic) monitor Program Select LL, Write Inhibit PP, Read X, and Read Inhibit RR in order to enable operation of the digital card. Output from Read Gate U17 is routed to the analog card to control the Data Bus Drivers.

WORD LIMIT SELECT

Word Limit is jumper-selected at JP10 on the digital card to 32, 64, 256, 512, 1024, or 2048. JP10 limits the address range of the Programmer through Word Limit line CC, according to the configuration of the PROM being programmed.

PAUSE TIMER

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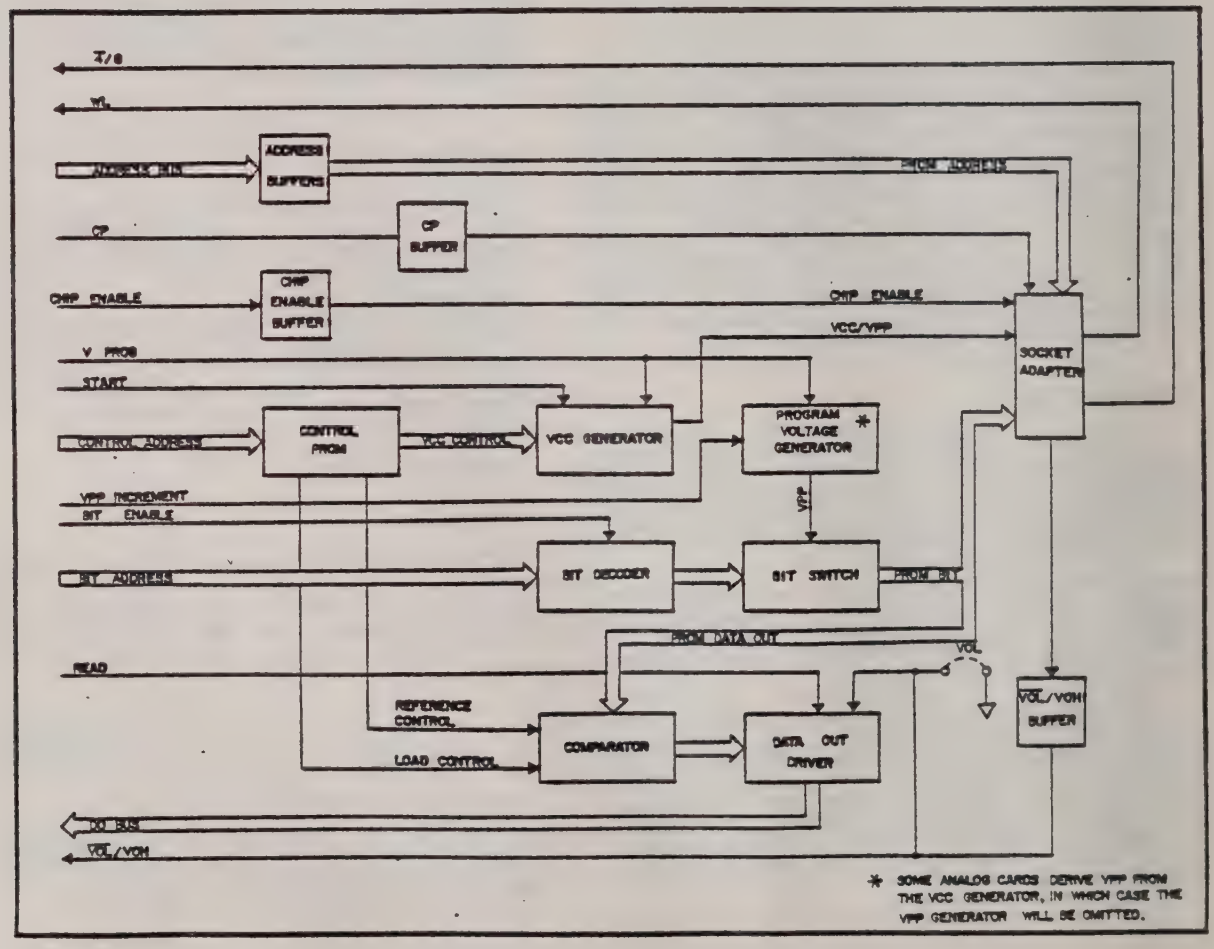
SELECT GATES

U17 and U18 (on schematic) monitor Program Select LL, Write Inhibit PP, Read X, and Read Inhibit RR in order to enable operation of the digital card. Output from Read Gate U17 is routed to the analog card to control the Data Bus Drivers.

WORD LIMIT SELECT

Word Limit is jumper-selected at JP10 on the digital card to 32, 64, 256, 512, 1024, or 2048. JP10 limits the address range of the Programmer through Word Limit line CC, according to the configuration of the PROM being programmed.

Figure 4-3. Analog Card Block Diagram.



ANALOG CARD CIRCUIT DESCRIPTION

Analog Card Operation

The analog card receives control signals from the digital card via J1, and from the Programmer via edge contacts. Figure 4-3 shows signal flow from analog card components to the PROM being programmed. Refer to the truth tables and timing diagrams at the rear of this manual for precise details about signal amplitudes and timing.

PROM bits are programmed individually within a given PROM word. Bit information arrives at analog card J1 and is used to drive the BIT DECODER U1. Decoder outputs enable the appropriate BIT PROGRAM SWITCHES and transfer program pulses to the bit lines of the PROM being programmed.

During the appropriate clock periods of the program cycle (see timing diagram) the bit switches are turned on, allowing the output of the Program Voltage Generator to reach the PROM bit lines.

Program Voltage Generator

The program voltage generator is a current limited regulator which supplies the programming voltage to the PROM outputs.

VCC Generator

The VCC generator is a current limited regulator with five selectable states: VCC KILL, VCC PROGRAM, VCC VERIFY FORWARD, VCC VERIFY REVERSE, and VCC READ.

On some dash numbers VCC KILL is used during the programming sequence to reduce the average power dissipation and improve programming yield. It also is used on some dash numbers in STOP, to remove VCC from the PROM socket during insertion and removal of the PROM.

VCC PROGRAM is selected while programming pulses are actually being applied to the PROM. After the programmer completes the forward and reverse programming passes, it enters the VERIFY mode. VCC VFY FWD and VCC VFY REV are used for parametric verification during the forward and reverse passes in the VERIFY mode. These levels are also used during the reading of the PROM when it is selected as an output device.

VCC READ is used during the reading of the PROM when it is selected as an input device. This level is also used during the READ portion of the programming cycle.

These levels are all selected via the CONTROL PROM U4 by signals from the digital card, and with the exception of VCC KILL they are adjustable by potentiometers R44-R47. Refer to the timing diagram for these voltage levels, and refer to the Calibration section for adjustment information.

Comparators

The comparators read the data at the output of the PROM under selectable load and threshold conditions.

The two thesholds are derived from voltage dividers under the control of PROM U4, and establish read thresholds for READ, PROGRAM, and VERIFY operations.

The load switch (depending on the dash number of the card set) provides the manufacturer's specified load during READ, isolation during PROGRAM for bits not being programmed, and/or specified parametric load during VERIFY. The load switch also is controlled via U4 by signals from the digital card.

DO Bus Drivers

These drivers pass the data from the comparators on to the DO Bus. When VOL is selected, either by shorting JP6 on the analog card or by the socket adapter taking J2-7 low, this data passes through with no inversion. That is, a programmed bit (below threshold on the comparators) yields a low on the DO Bus. If, however, VOH is selected by JP6 open or by J2-7 high, the data is inverted. In this case a programmed bit (above threshold on the comparators) is inverted by the bus drivers and again appears as a low on the bus.

$\overline{\text{VOL}}$/VOH Buffer

Some dash number card sets are capable of programming both VOL and VOH PROMs by leaving JP6 open and allowing the socket adapter to pull J2-7 low for the VOL parts. For some existing VOL socket adapters, J2-7 is connected to the active high CHIP ENABLE of the PROM being programmed. If this buffer were not present, shorting JP6 to select the VOL mode would disable the PROM. This buffer provides the necessary isolation for CHIP ENABLE in this case.

Warranty

Data I/O equipment is guaranteed against defects in materials and workmanship. The warranty period is ninety days on new equipment, and thirty days on used equipment. Warranty period begins on receipt of equipment. Data I/O will repair or replace, at Data I/O's option, any equipment found to be defective within the warranty period.

Warranty service will be provided by Data I/O within a reasonable amount of time after notification by the purchaser to Data I/O of equipment malfunction. This service shall not apply to equipment that has been subjected to abuse, misuse, negligence or accident as determined by Data I/O, or to which any modifications, alterations, or attachments have been made without written authorization from Data I/O, nor shall it apply if the equipment is installed or operated in an environment containing excessive dirt, dust, moisture, fumes, humidity, or extremes of temperature.

This warranty policy is in lieu of all other warranties, expressed or implied, unless standard warranty exceptions are granted by Data I/O in writing.

Service

After expiration of the warranty period, service and repairs are billed at standard hourly rates, plus expenses, portal-to-portal. Time and one-half rate will apply outside of normal working hours.

Cost of engineering (where applicable) and parts, plus the cost of installation is billed at standard service labor rates when implementing approved, customer requested modifications.

Shipment

Products returned to Data I/O should be accompanied by a letter or enclosure explaining the reason for their return and action requested of Data I/O. Please include the following additional information: Company name and address; attention of; method of shipment desired; serial number; date of purchase; billing information, and purchase order number.

All products returned to Data I/O must be sent prepaid F.O.B. The warranty is voided if returned items are not packaged by the customer in original packing material, or in other Data I/O approved containers. If reshipment method is not specified by customer, Data I/O will return products by most expedient shipping method, F.O.B. our plant.

Ship returned equipment to:

DATA I/O CORPORATION
1297 N.W. Mall
Issaquah, Washington 98027

From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

Parts Ordering

Orders for parts should contain the following information:

a. Description of part(s) and Data I/O part number(s).
b. Quantity of each item to be ordered.
c. Equipment serial number and model number.
d. Corporate name of firm.
e. Shipping address of firm, including zip code.
f. Full name of person ordering the part(s).
g. To whose attention the part(s) are to be shipped.
h. Billing information.
i. Purchase order number.
j. Method of shipment.

Please send all parts orders to:

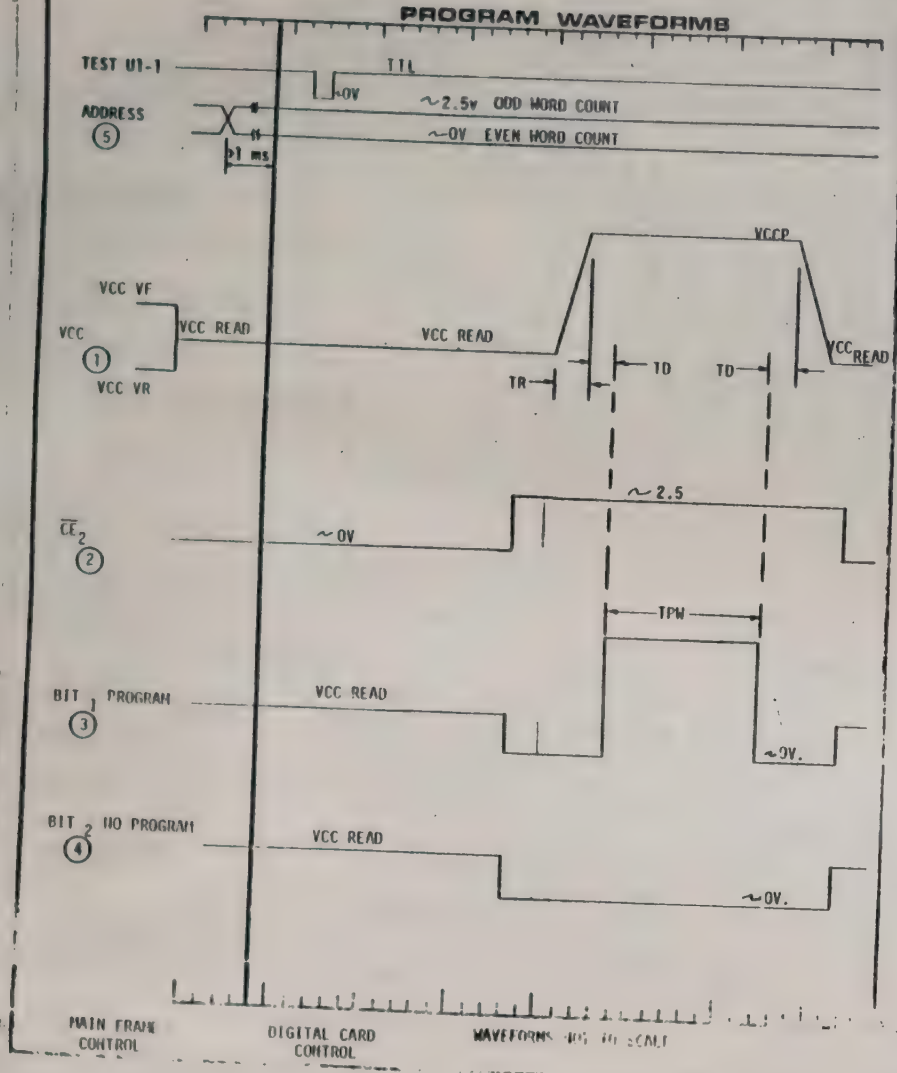
DATA I/O CORPORATION
P O Box 308
Issaquah, Washington 98027

From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

DATE	BY	REVISION RECORD	DR	CK
7/1	P	CN# 1997	DS	DS
7/15	R	ECN# 2315	KJ	KJ
8/28	S	ECN# 2369	KJ	DB

PROGRAM WAVEFORMS



NOTES

DIGITAL CARD JUMPERS
- JP1 = OPEN
- JP2 = SHORT
- JP3 = SHORT
- JP4 = SHORT
- JP5 = SHORT
- JP6 = SHORT
- JP7C = 8 PULSE REJECT
- JP7M = 1 PULSE REJECT
- JP8 = OPEN
- JP9 = N
- JP10 = WORD LIMIT =2048
- JP11 = OPEN

ABORT TIMER = JP1 = NOT USED

PAUSE TIMER (CR2) = NOT USED

WAVEFORM VARIABLES

PROGRAMMING DUTY CYCLE 34%

TD ≥ 10 μ sec.

TPW = 100 ± 10 μ sec.

TR = 2-10uS
VCC VR = 4.5 ± .2 volts
VCC READ = 5.0 ± .2 volts

VCC VF = 5.5 ± .2 volts

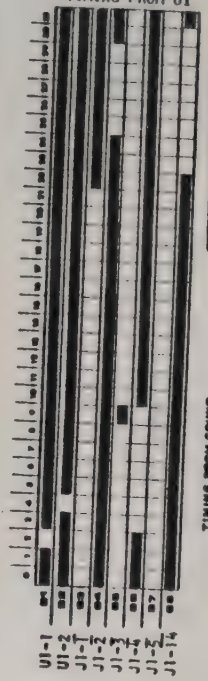
VCCP = VOP = 12.00 ± .25 volts

○ THESE WAVEFORMS CORRESPOND TO CALLOUTS ON THE CALIBRATION CHART. SWITCH S2 AND S3 OF THE UNIVERSAL CALIBRATOR TO INDICATED POSITIONS TO OBTAIN WAVEFORMS. REFER TO PERFORMANCE CHECK SECTION OF MANUAL FOR DETAILED STEPS.

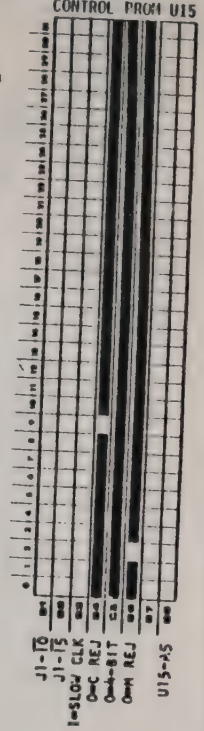
TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)

TIMING PROM U1

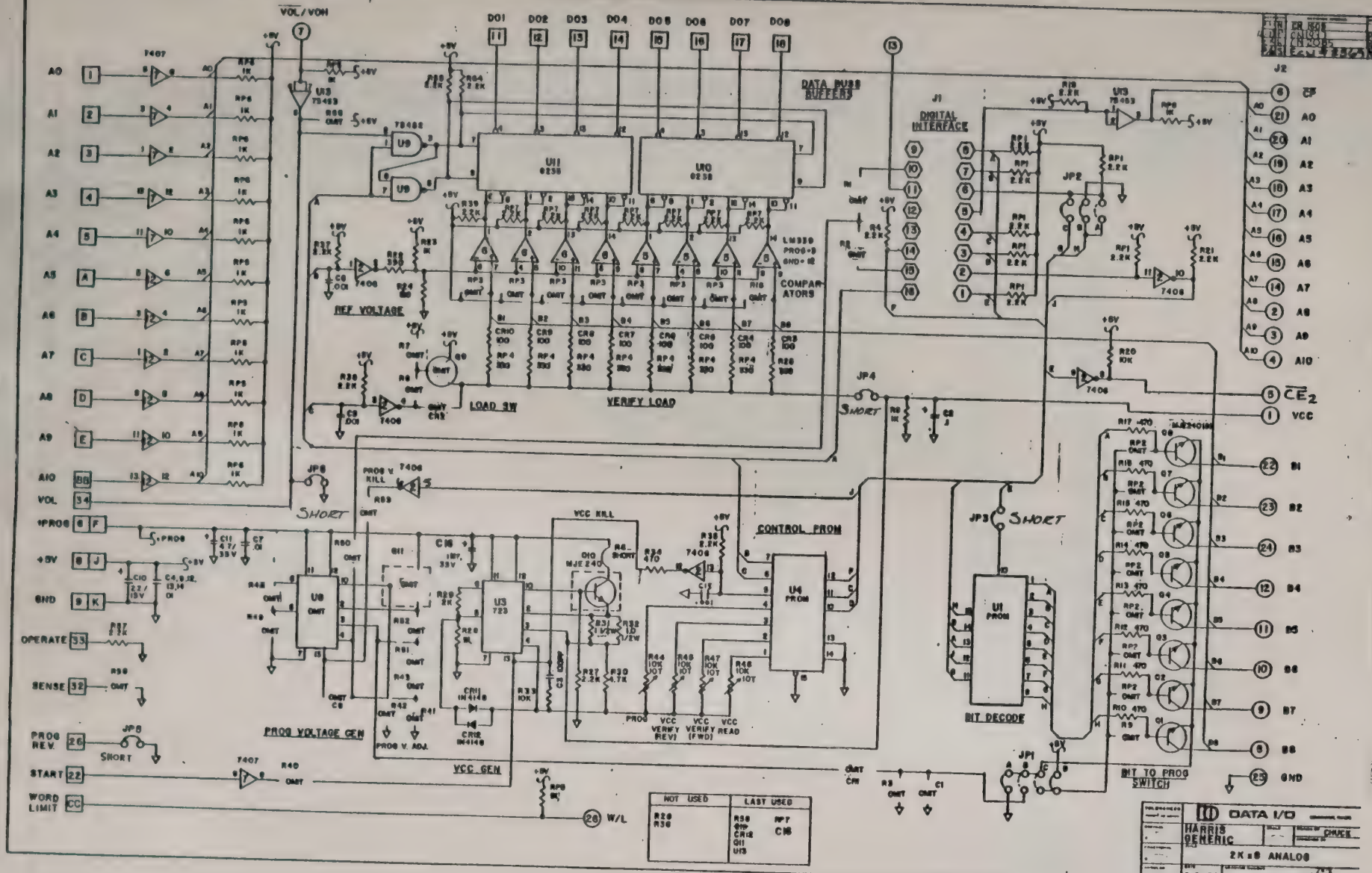


CONTROL PROM U15

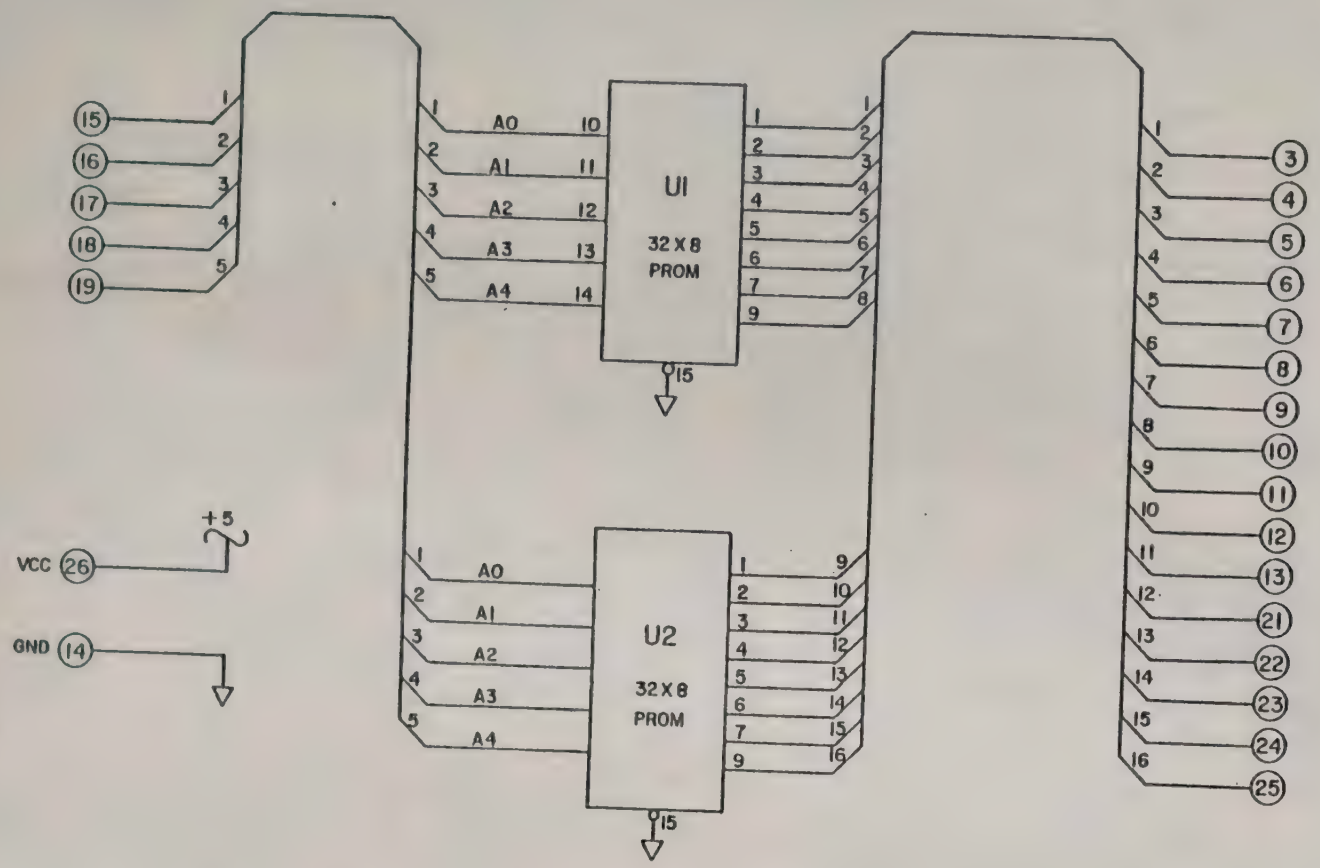


DATA I/O (ISSAQUAH, WASH.)

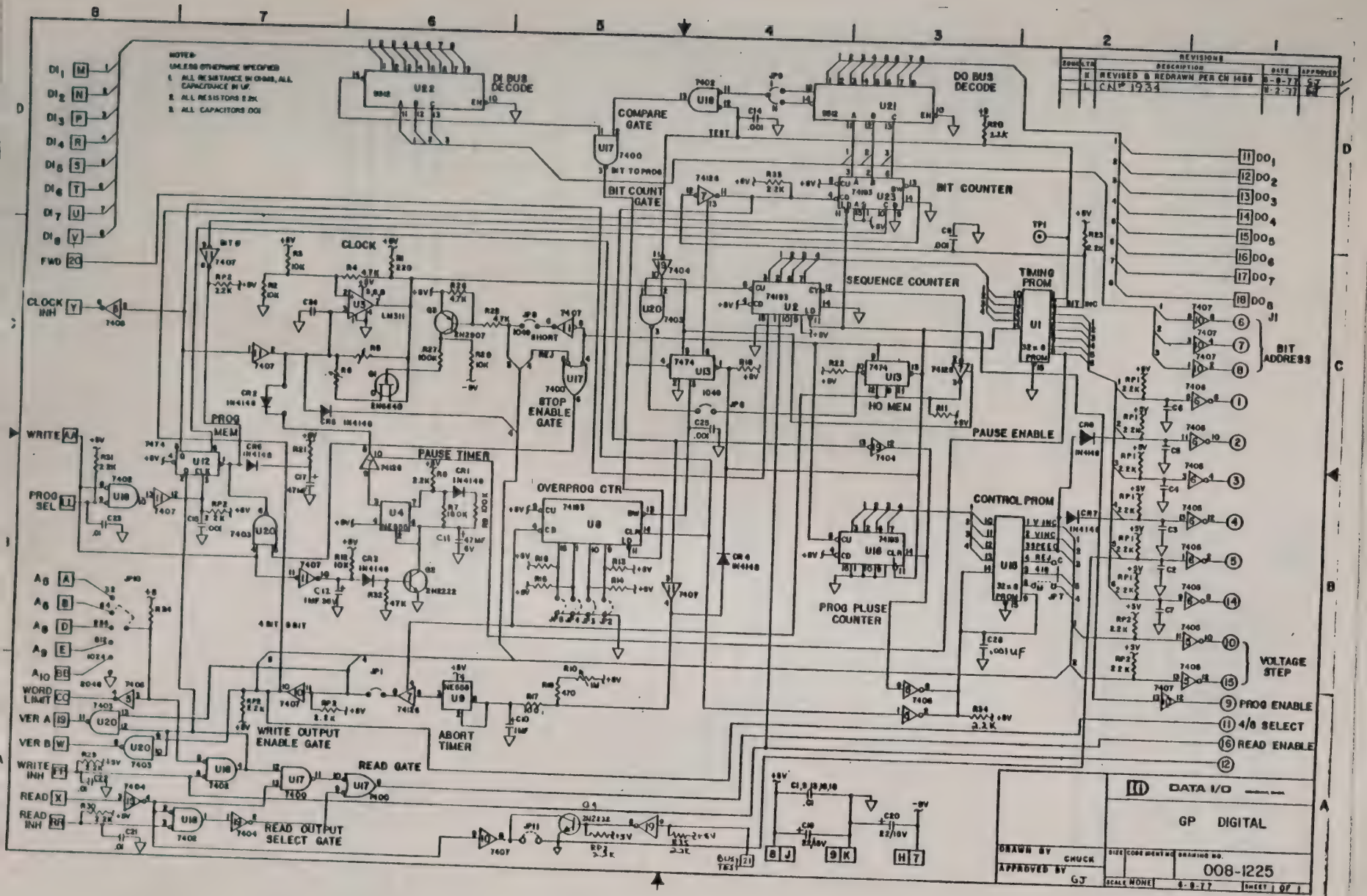
TIMING DIAGRAM	DRAWN BY K.J.
	CHK'D BY G.T.
TITLE: HARRIS GENERIC	
DATE: 9-2-76	DRAWING NUMBER: 007-1063-4


VOL/VOH
DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8
DATA BUS BUFFERS
DIGITAL INTERFACE
J1
J2
U11 8238
U10 8238
COMPARATORS
REF VOLTAGE
LOAD SW
VERIFY LOAD
JP4 SHORT
JP6 SHORT
JP8 SHORT
JP3 SHORT
CONTROL PROM
U4 PROM
U1 PROM
BIT DECODE
BIT TO PROG SWITCH
PROG VOLTAGE GEN
VCC GEN
VCC KILL
PROG V KILL
PROG V. ADJ.
VCC VERIFY (REV)
VCC VERIFY (FWD)
VCC READ
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
VOL
+PROG
+5V
GND
OPERATE
SENSE
PROG REV.
START
WORD LIMIT
W/L
B1
B2
B3
B4
B5
B6
B7
B8
CE2
VCC
GND
NOT USED
LAST USED
DATA I/O
HARRIS GENERIC
2K x 8 ANALOG
9-1-77
008-1083-4

DATE	SYM	REVISION RECORD	DR
11-15-75	A	RELEASE	



TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH		
DECIMAL ±		SCALE	DRAWN BY G. ROPPE
FRACTIONAL ±	TITLE PLUG IN ADAPTER (UNIVERSAL CALIBRATOR)		APPROVED BY
ANGULAR °	DATE 10-15-75	DRAWING NUMBER 008-1072	


NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE IN OHMS, ALL CAPACITANCE IN UF.
2. ALL RESISTORS 2.2K
3. ALL CAPACITORS .001
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
K REVISED & REDRAWN PER CN 1488 8-9-77 GJ
L CN# 1934 9-2-77
DI BUS DECODE
DO BUS DECODE
COMPARE GATE
BIT COUNT GATE
BIT COUNTER
SEQUENCE COUNTER
TIMING PROM
CLOCK
CLOCK INH
FWD
WRITE
PROG SEL
PROG MEM
PAUSE TIMER
STOP ENABLE GATE
OVERPROG CTR
HO MEM
PAUSE ENABLE
CONTROL PROM
PROG PLUSE COUNTER
BIT ADDRESS
VOLTAGE STEP
PROG ENABLE
4/8 SELECT
READ ENABLE
WORD LIMIT
VER A
VER B
WRITE INH
READ
READ INH
WRITE OUTPUT ENABLE GATE
ABORT TIMER
READ GATE
READ OUTPUT SELECT GATE
DATA I/O
GP DIGITAL
DRAWN BY CHUCK
APPROVED BY GJ
008-1225
SCALE NONE
8-9-77
SHEET 1 OF 1

INSPECTION

Data I/O certifies that this equipment was shipped in compliance with Data I/O's quality assurance, burn-in, calibration, and performance check procedures.

*By _____
Q.C. Inspection

PART NO. _____

TEST	CHECK-OFF*
QUALITY ASSURANCE	✓
BURN-IN	✓
CALIBRATION	✓
PERFORMANCE	✓
PACKAGING	✓

Retain This Portion for Your Files

Reader Comments

The manual's completeness, accuracy, organization, usability, and readability: _____

Did you find errors in this manual? _____

How can this manual be improved? _____

Other comments: _____

Name _____

Company _____

Department _____ M/S _____

Address _____

City _____ State _____ Zip _____

Phone _____ Ext. _____

Manual or Part No. _____

WARRANTY / REGISTRATION

Please return this card to Data I/O within five days

Did the packaging of this equipment exhibit any outward signs of physical damage? . . . . . YES ☐ NO ☐
Did this equipment arrive intact, without loose parts or cable damage? . . . . . YES ☐ NO ☐
Did the equipment operate on power-up? . . . . . YES ☐ NO ☐
Did you attain adequate system performance? . . . . . YES ☐ NO ☐
Were any electrical adjustments required? . . . . . YES ☐ NO ☐
If you required assistance, was a local Data I/O representative contacted? . . . . . YES ☐ NO ☐

Comments – _____

Name _____ Title _____

Department _____ M/S _____

Company _____

Address _____

City _____ State _____ Zip _____ Phone ( ) _____

Model or Description _____ Serial or Part No. _____

Date Received _____

WARRANTY

Data I/O equipment is guaranteed against defects in materials and workmanship. The warranty period is ninety days on new equipment, and thirty days on used equipment. Data I/O will repair or replace, at Data I/O's option, any equipments found to defective within the warranty period.

Warranty service will be provided by Data I/O within a reasonable amount of time after notification by the purchaser to Data I/O of equipment malfunction. This service shall not apply to equipment that has been subjected to abuse, misuse, negligence or accident, as determined by Data I/O, or to which any modifications, alterations, or attachments have been made without written authorization from Data I/O, nor shall it apply if the equipment is installed or operated in an environment containing excessive dirt, dust, moisture, fumes, humidity, or extremes of temperature.

This warranty policy is in lieu of all other warranties, expressed or implied, unless standard warranty exceptions are granted by Data I/O in writing.

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